What is claimed is:

1. A method for making an integrated circuit dual damascene, wherein the integrated circuit dual damascene is formed by an anti-reflection coating layer that is soluble in a development liquid, and the method for making the self-aligned dual damascene comprises:

providing a substrate, wherein an insulating dielectric layer is deposited on the substrate, the insulating dielectric layer has a first dielectric layer, a second dielectric layer, and a middle dielectric layer, and the middle dielectric layer is between the first dielectric layer and the second dielectric layer;

forming a first photo-resist layer on the insulating dielectric layer;

forming the anti-reflection coating layer on the first photo-resist layer;

forming a second photo-resist layer on the anti-reflection coating layer;

exposing the second photo-resist layer through a first photo mask to define an interconnect pattern in the second photo-resist layer;

proceeding with wet development to the second photo-resist layer and the anti-reflection coating layer;

exposing the first photo-resist layer through a second photo mask to define a window pattern in the first photo-resist layer;

proceeding with wet development to the first photo-resist layer;

using the first photo-resist mask as mask to etch the second dielectric layer below the first photo-resist layer, and transferring the defined window pattern of the first photo-resist layer to the second dielectric layer;

using the first photo-resist layer as mask to etch the middle dielectric layer below the second dielectric layer, and transferring the defined window pattern of the first photo-resist layer to the middle dielectric layer;

dry etching to the second photo-resist layer to extend the defined interconnect pattern to the second dielectric layer;

etching the insulating dielectric layer, thereby transferring the defined interconnect pattern of the first photo-resist layer to the second dielectric layer to form an interconnect trench, and automatically transferring the defined window pattern of the middle dielectric layer to the first dielectric layer to form a window;

removing all the photo-resist layers; and

depositing a metal layer into the interconnect trench and the window to form a dual damascene structure.

2. The method for making the integrated circuit dual damascene according to claim 1, wherein the method for planarizing the insulating dielectric layer is chemical mechanical polishing.

3. The method for making the integrated circuit dual damascene according to claim 1, wherein the first dielectric layer of the insulating dielectric layer is made of phosphosilicate glass, and the thickness of the first dielectric layer is about 0.3 m to 0.7 m.

4. The method for making the integrated circuit dual damascene according to

claim 1, wherein the middle dielectric layer is made of silicon nitride, and the thickness of the middle dielectric layer is about 500 to 2000 .

5. The method for making the integrated circuit dual damascene according to claim 1, wherein the second dielectric layer of the insulating dielectric layer is made of phosphosilicate glass, and the thickness of the first dielectric layer is about 0.3 m to 0.7 m.

6. The method for making the integrated circuit dual damascene according to claim 1, wherein the first photo-resist layer is made of a positive chemically-amplified resist.

7. The method for making the integrated circuit dual damascene according to claim 1, wherein the thickness of the first photo-resist layer is about 0.40 m to 0.90m.

8. The method for making the integrated circuit dual damascene according to claim 1, wherein the anti-reflection coating layer is water-soluble.

9. The method for making the integrated circuit dual damascene according to claim 1, wherein the refractive index of the anti-reflection coating layer is about 1.4 to 2.0.

10. The method for making the integrated circuit dual damascene according to

claim 1, wherein the thickness of the anti-reflection coating layer having the spacer is about 200 to 700 .

11. The method for making the integrated circuit dual damascene according to claim 1, wherein the second photo-resist layer is made of a positive chemically-amplified resist.

12. The method for making the integrated circuit dual damascene according to claim 1, wherein the thickness of the second photo-resist is about 0.40 m to 0.90 m.

13. The method for making the integrated circuit dual damascene according to claim 1, wherein the first photo mask thereon has a defined negative photo-resist interconnect pattern of clear tone.

14. The method for making the integrated circuit dual damascene according to claim 1, wherein the development solution used in wet development to the second photo-resist layer and the anti-reflection coating layer is a solution comprising 2.38 % TMAH development liquid, and is completed after being kept still for 45 seconds to 70 seconds.

15. The method for making the integrated circuit dual damascene according to claim 1, wherein the second photo mask thereon has a defined positive photo-resist interconnect pattern of dark tone.

16. The method for making the integrated circuit dual damascene according to claim 1, wherein the development solution used in wet development to the first photo-resist layer is a solution comprising 2.38 % TMAH development liquid, and is completed after being kept still for 45 seconds to 70 seconds.

17. The method for making the integrated circuit dual damascene according to claim 1, wherein the first photo-resist mask is used as mask to etch the second dielectric layer below the first photo-resist layer, and a high density plasma oxide etcher is used to transfer the defined window pattern of the first photo-resist layer to the second dielectric layer, wherein the etching condition comprises Ar, CHF_3, and C_4F_8, and the flow rates are about 50 sccm to 150 sccm, about 10 sccm to 50 sccm, and about 0 to 22 sccm, respectively.

18. The method for making the integrated circuit dual damascene according to claim 1, wherein the first photo-resist mask is used as mask to etch the middle dielectric layer below the second dielectric layer, and a high density plasma silicon nitride etcher is used to transfer the defined window pattern of the first photo-resist layer to the middle dielectric layer, wherein the etching condition comprises Ar, CHF_3, and CF_4, and the flow rates are about 50 sccm to 150 sccm, about 0 sccm to 100 sccm, and about 0 to 50 sccm, respectively.

19. The method for making the integrated circuit dual damascene according to

claim 1, wherein a dry etching is used to dry etch the second photo-resist to extend the defined interconnect pattern to the second dielectric layer, wherein the etching condition comprises O_2, He, and CF_4, and the flow rates are about 10 sccm to 250 sccm, about 40 sccm to 80 sccm, and about 0 to 50 sccm, respectively.

20. The method for making the integrated circuit dual damascene according to claim 1, wherein the insulating dielectric layer is etched to transfer the defined interconnect pattern to the second dielectric layer, and a high density plasma oxide etcher is used to form an interconnect trench and to automatically transfer the defined window pattern of the middle dielectric layer to the first dielectric layer to form a contact window, wherein the etching condition comprises Ar, CHF_3, and C_4F_8, and the flow rates are about 50 sccm to 150 sccm, about 10 sccm to 50 sccm, and about 0 to 22 sccm, respectively.

21. The method for making the integrated circuit dual damascene according to claim 1, wherein the method for removing the photo-resist layer is an oxygen plasma ashing method and a wet stripping method, wherein H_2SO_4, H_2O_2, and NH_4OH are used in the wet stripping method.

22. The method for making the integrated circuit dual damascene according to claim 1, wherein the metal material used to deposit to form the dual damascene structure is freely selected from a metal group, wherein the metal group is made from Cu metal and Al/Cu alloy.

23. A method for making an integrated circuit dual damascene, wherein the defined dual damascene metal pattern is formed by an anti-reflection coating layer that is soluble in a development liquid, and the method for making the self-aligned dual damascene comprises:

providing a substrate, wherein the substrate has an insulating dielectric layer, the insulating dielectric layer comprises a top dielectric layer, a bottom dielectric layer, and a middle dielectric layer, the middle dielectric layer is between the top dielectric layer and the bottom dielectric layer;

forming a first photo-resist layer on the insulating dielectric layer;

forming an anti-reflection coating layer in a spacer;

forming a second photo-resist layer on the first photo-resist layer;

proceeding with interconnect definition to the second photo-resist layer by a first mask;

proceeding with window definition to the first photo-resist layer by a second mask;

transferring the defined window pattern of the first photo-resist layer to the top dielectric layer and the middle dielectric layer of the insulating dielectric layer by etching;

transferring the defined interconnect pattern of the second photo-resist layer to the second dielectric layer to form an interconnect trench, and automatically transferring the defined window pattern of the middle dielectric layer to the first dielectric layer to form an interconnect window;

removing the photo-resist layer; and

depositing a metal layer into the trench and the window to form a dual damascene structure, and planarizing the mixed layer.

24. The method for making the integrated circuit dual damascene according to claim 23, wherein the mixed layer is made of phosphosilicate glass.

25. The method for making the integrated circuit dual damascene according to claim 23, wherein the middle dielectric layer is made of silicon nitride, and the thickness of the middle dielectric layer is about 500 to 2000 .

26. The method for making the integrated circuit dual damascene according to claim 23, wherein the first photo-resist layer is made of a chemically-amplified resist.

27. The method for making the integrated circuit dual damascene according to claim 23, wherein the anti-reflection coating layer is water-soluble.

28. The method for making the integrated circuit dual damascene according to claim 23, wherein the first mask is cleat tone mask, and the interconnect pattern is defined by negative photo-resist.

29. The method for making the integrated circuit dual damascene according to claim 23, wherein the second mask is dark tone mask, and the interconnect pattern is

defined by positive photo-resist.

30. The method for making the integrated circuit dual damascene according to claim 23, wherein the defined interconnect pattern of the photo-resist layer is transferred to the second dielectric layer, a high density plasma oxide dry etching is used to form an interconnect trench, and the defined window pattern of the middle dielectric layer is automatically transferred to the first dielectric layer to form an interconnect window, wherein the etching condition comprises Ar, CHF_3, and C_4F_8, and the flow rates are about 50 sccm to 150 sccm, about 10 sccm to 50 sccm, and about 0 to 20 sccm, respectively.

31. The method for making the integrated circuit dual damascene according to claim 23, wherein the metal material used to deposit to form a dual damascene structure is freely selected from a metal group, wherein the metal group is made from Cu metal and Al/Cu alloy.